Research on Moisture Barrier Technology and Reliability Evaluation of Flip-chip Circuit with Organic Substrate

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***Abstract*—Flip-chip circuits with organic substrate are widely used in modern microelectronic packaging due to their high-density interconnections and low-cost advantages. However, the hygroscopic properties of the polymer materials used in package process lead to interfacial delamination and electrochemical corrosion in humid environments, severely limiting their reliability under high-temperature and high-humidity conditions. To enhance the reliability of flip-chip circuits with organic substrate in humid environment, this study employed two methods—nano-coated and Parylene-coated—to shield the circuits. Moisture barrier effectiveness was comprehensively assessed through moisture absorption weight gain tests, heavy water tracing combined with Time-of-flight Secondary Ion Mass Spectrometry (ToF-SIMS) analysis, and Moisture Sensitivity Level 1 (MSL 1) preconditioning (reflow soldering with 260°C peak temperature). Both protective layers significantly inhibit moisture penetration, with saturated moisture absorption rates of 0.207% for the nano-coated sample, 0.224% for the Parylene-coated sample and 0.256% for the unprotected sample. The protective layers did not alter the diffusion pathway but effectively prolonged the permeation process. Heavy water tracing revealed a one-order-of-magnitude reduction in D^- intensity at the interfaces of both protected samples, with the nano-coated showing slight superiority over Parylene due to its molecular-level hydrophobic structure. After the MSL 1 preconditioning, both barrier layer prevented the formation of microcracks at the interface between the chip edge and the underfill. The underfill itself did not crack, and the adhesion between the underfill and both the solder mask and the polyimide (PI) remained intact. Barrier layers enhance moisture resistance through distinct mechanisms: nanoparticle coatings rely on nanoporous barrier effects and surface hydrophobicity, while Parylene leverages its conformal and pin-hole free coating. These findings provide reference and experimental data support for the characterization and optimization of moisture barrier technology for flip-chip circuits with organic substrate.**

Keywords—moisture barrier, nano-coated, parylene-coated, flip-chip circuit with organic substrate

I. Introduction

As microelectronic packaging technology advances toward higher density, flip chip technology has become a key choice for advanced packaging due to its superior electrical performance and interconnect density. Simultaneously, to meet demands for small size, and lightweight development, organic substrate is gradually replacing traditional ceramic substrate in high reliability application areas. However, the hygroscopic nature of underfill materials, core layer materials, and build-up layer materials used in flip-chip circuits on organic substrates poses significant challenges for applications in humid environments[1-2]. The impact of moisture on flip-chip circuits with organic substrate manifests primarily through physical damage and chemical corrosion. Physical damage is mainly caused by interfacial delamination and crack formation induced by moisture-heat stress and vapor pressure. When the underfill absorbs moisture, high temperatures during reflow soldering rapidly vaporize the moisture, generating vapor pressure. This pressure concentrates at material interfaces. When it exceeds the interfacial bonding strength, cracks initiate and propagate between the chip and underfill. Chemical corrosion primarily stems from electrochemical reactions triggered by moisture penetration into circuitry. When ambient humidity permeates through organic substrate materials or interfacial defects into internal circuits, it ionizes under powered operating conditions to produce hydroxide ions. These reactive ions undergo electrochemical reactions with microbumps, redistribution layers, and internal chip metal interconnects, forming corrosion products like metal hydroxides, thus compromising the long-term reliability of flip-chip circuits on organic substrates.

In the field of moisture barrier technology, researchers have developed various protective technologies, primarily categorized into material modification, structural optimization, and surface coating. Among these, surface coating technology has emerged as a research hotspot due to its simplicity of implementation and significant effectiveness. Parylene films are typically prepared using vacuum vapor deposition methods and exhibit extremely low moisture transmission rates and outstanding barrier properties. The coating process involves the deposition and polymerization of active di-free radical small molecules on the surface of circuit components. These gaseous small molecules can permeate into any minute gap on the substrate, forming a uniform protective film free of pinholes[3-5]. Nano-coating technology represents another advanced protective approach. Through specialized synthesis and application processes of nanomaterials, it forms a molecular-level protective layer on circuit surfaces. While most studies have focused on other fields, high-reliability flip-

采用有机基板的倒装芯片电路的防潮技术及可靠性评估研究

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***摘要*——采用有机基板的倒装芯片电路因其高密度互连和低成本优势而广泛应用于现代微电子封装领域。然而，封装过程中所用聚合物材料的吸湿性会导致在潮湿环境中出现界面剥离和电化学腐蚀现象，从而严重限制了其在高温高湿条件下的可靠性。为提高采用有机基板的倒装芯片电路在潮湿环境下的可靠性，本研究采用两种方法——纳米涂层法和聚对二甲苯涂层法——对电路进行屏蔽处理。通过吸湿增重测试、重水示踪结合飞行时间二次离子质谱（ToF-SIMS）分析以及湿度敏感性等级1（MSL 1）预处理（采用峰值温度为260°C的回流焊工艺）对阻湿性能进行了全面评估。两种保护层均能显著抑制水分渗透：纳米涂层样品的饱和吸湿率分别为0.207%，聚对二甲苯涂层样品为0.224%，而未作保护处理的样品为0.256%。保护层并未改变水分扩散路径，但有效延长了渗透过程。重水示踪实验表明，两个受保护样品界面处的D-强度均降低了一个数量级；由于纳米涂层具有分子级疏水结构，其性能略优于聚对二甲苯涂层。经过MSL 1预处理后，两种阻隔层均有效防止了芯片边缘与灌封层之间界面处出现微裂纹。灌封层本身未发生开裂，且灌封层与阻焊层及聚酰亚胺（PI）之间的粘附力保持完好。阻隔层通过不同的机制增强耐湿性：纳米颗粒涂层依赖于纳米多孔阻隔效应及表面疏水性，而聚对二甲苯涂层则利用其具有高保形性且无针孔的涂覆特性。这些研究结果为针对采用有机基板的倒装芯片电路设计及优化耐湿性阻隔技术提供了参考依据与实验数据支持。**

***关键词*——防潮层、纳米涂层、聚对二甲苯涂层、带有机基板的倒装芯片电路**

I. 引言

随着微电子封装技术向更高密度方向发展，倒装芯片技术因其卓越的电气性能和高互连密度而成为先进封装领域的首选方案。与此同时，为满足小型化、轻量化开发的需求，有机基板正逐渐取代传统陶瓷基板，广泛应用于高可靠性应用场景中。然而，用于有机基板上倒装芯片电路的灌封材料、芯层材料及堆叠层材料所具有的吸湿性，给在潮湿环境中的应用带来了显著挑战[1-2]。水分对采用有机基板的倒装芯片电路的影响主要表现为物理损伤和化学腐蚀两种形式。物理损伤主要由水分-热应力及蒸汽压引发的界面分层和裂纹形成所导致；当灌封材料吸收水分时，回流焊过程中的高温会迅速使水分汽化，从而产生蒸汽压，该压力会集中于材料界面处。当界面结合强度被超过时，裂纹会在芯片与填充材料之间产生并扩展。化学腐蚀主要源于水分渗入电路所引发的电化学反应。当环境湿度渗透至有机基板材料或通过界面缺陷进入内部电路时，在带电工作条件下，这些水分会电离产生氢氧根离子。这些活性离子与微凸点、再分布层以及芯片内部金属互连结构发生电化学反应，形成金属氢氧化物等腐蚀产物，从而影响有机基板上倒装芯片电路的长期可靠性。

在防潮技术领域，研究人员开发了多种保护性技术，这些技术主要可分为材料改性、结构优化和表面涂层三大类。其中，表面涂层技术因其实施简便且防护效果显著而成为当前研究热点。聚对二甲苯薄膜通常采用真空气相沉积法制备，其防潮渗透率极低，且具有优异的阻湿性能。该涂层工艺涉及将活性双自由基小分子沉积并聚合于电路元件表面；这些气态小分子可渗透至基材上的任何微小间隙中，从而形成一层无针孔的均匀保护膜[3-5]。纳米涂层技术则是另一种先进的保护性方案——通过纳米材料的特殊合成与应用工艺，在电路表面构建一层分子级保护层。尽管目前大多数研究聚焦于其他领域，但采用有机基材的高可靠性倒装芯片电路如今也亟

chip circuit with organic substrate now also face the need for moisture barrier.

This study employs two advanced protective processes: nano-coating and Parylene-coating. Nano-coating provides barrier through molecular-level hydrophobic shielding, while Parylene-coating forms a dense barrier film via chemical vapor deposition. To systematically evaluate protective efficacy, three validation methods were employed: Moisture absorption weight gain tests quantitatively analyzed vapor barrier performance; Heavy water tracer tests visually revealed moisture diffusion rate by scanning D ion concentration distribution at the substrate-underfill interface. MSL 1 preconditioning combined with three 260°C reflow soldering tests examined interfacial delamination and cracking; This study aims to provide an effective moisture barrier solution for flip-chip circuits with organic substrate. Through systematic experimental design and multi-perspective evaluation methods, it offers theoretical basis and practical guidance for the long-term stable operation of high-reliability electronic equipment in harsh environments.

II. EXPERIMENT

A. Materials and Equipment

The subject of this study is flip-chip circuits with organic substrates. The chip dimensions were 15mm×19mm, and the substrate dimensions were 42mm×42mm. The protective materials used in the experiment include nano-coated material primarily composed of fluoropolymer with 10% solid content, dissolved in organic solvent and Parylene material with 99.9% purity. Experimental equipment consist of a precision electronic balance, a constant temperature and humidity chamber, a reflow soldering oven, a secondary ion mass spectrometer, and a scanning electron microscope.

B. Sample Preparation

According to the IPC/JEDEC J-STD-033 Joint Industry Standard, all experimental samples were baked at 125°C for 24h to remove residual internal moisture. Then they were randomly divided into three groups: the unprotected group, the nano-coated group, and the Parylene-coated group. The nano-coated group employed a dip-and-brush process: circuits were immersed in the nano-coating solution for 3 seconds, followed by 12h of curing at room temperature. The thickness of the nano-coating is relatively thin, and the morphology is not very obvious under SEM observation as shown in Fig. 1. The Parylene group employed a vacuum chemical vapor deposition process to deposit a uniform film approximately 13μm thick onto the circuit surface. Fig. 2 clearly shows a dense parylene film on the sample surface. Subsequent experimental procedures described in this study were performed within 72h after the sample preparation was completed.

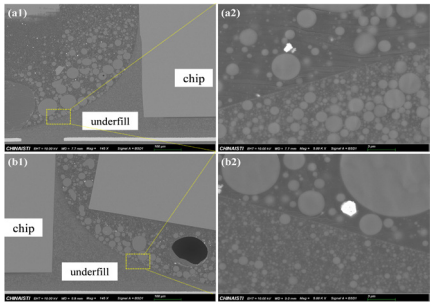

Fig. 1. SEM morphology of the nano-coating (a) Left side (b) Right side.

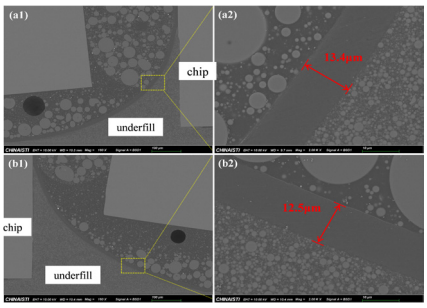

Fig. 2. SEM morphology of the Parylene-coating (a) Left side (b) Right side.

C. Trial Protocol

Moisture Absorption Test: Place three sets of samples in a constant temperature and humidity chamber at 85°C/85% RH. Measure mass changes using a precision electronic balance. The moisture absorption test schedule is set as follows: Weighing occurs at 0h, 1h, 2h, 4h, 6h, 8h, 10h, and 12h during the initial 12h. Weighing occurs every 12h between 12h and 204h. After 204h, weighing occurs every 24h until moisture absorption reaches saturation.

D_2O Isotope Tracing Test: Three sets of samples were placed in an 85°C/85% RH environment filled entirely with D_2O for 1 h. After removing the sample from the test chamber, grind the substrate flat from the rear side until the substrate-underfill interface is exposed, as shown in Figure 4. ToF-SIMS was employed to analyze at the interface, measuring the distribution of H and D ion concentration over a scan area of 500μm×8000μm. Tof-SIMS detects all H and D ion present in the sample, encompassing both H and D ion from the sample's constituent molecules and D ion diffused into the sample during the one-hour HAST test. In nature the D-to-H (D/H) ratio is about 1.55×10^{-4} [6]. To isolate the influence of bumps on the scanning of D ion signals, this set of experiments required the use of bump-reduced packaging samples. Only 50 bumps were manually placed at the four corners and the center of the chip, while all other packaging processes remained consistent.

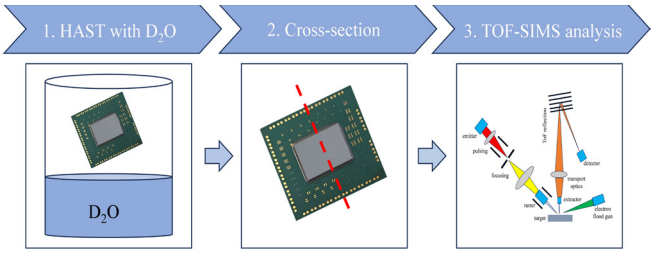

Fig. 3. Experimental flow of D_2O isotope tracing method.

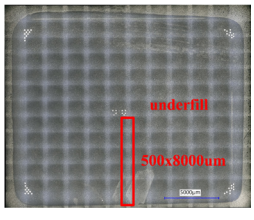

Fig. 4. Cross section of the scan area.

MSL 1 preconditioning and Reflow Soldering Test: In accordance with JEDEC J-STD-020 standards, three sample groups underwent MSL 1 preconditioning (85°C/85%RH, 168 h). Within 4h after moisture absorption completion, three reflow soldering cycles were performed at a peak temperature

需具备防潮保护功能。

本研究采用两种先进的防护工艺：纳米涂层与聚对二甲苯涂层。纳米涂层通过分子级疏水屏蔽作用形成阻隔层，而聚对二甲苯涂层则通过化学气相沉积法形成致密阻隔膜。为系统评估防护效能，本研究采用了三种验证方法：水分吸收增重试验对气密性阻隔性能进行定量分析；重水示踪试验通过扫描基材-下填充界面处的D离子浓度分布，直观揭示水分扩散速率；MSL 1预处理结合三次260°C回流焊测试，用于检测界面分层与开裂现象；本研究旨在为采用有机基材的倒装芯片电路提供有效的防潮解决方案。通过系统化的实验设计与多维度评估方法，本研究为高可靠性电子设备在严苛环境下的长期稳定运行提供了理论依据与实践指导。

II. 实验

A. 材料与设备

本研究对象为采用有机基板制造的倒装芯片电路。芯片尺寸为 15 mm × 19 mm，基板尺寸为 42 mm × 42 mm。实验中使用的保护材料包括：一种主要由固含量为 10% 的氟聚合物溶解于有机溶剂中制成的纳米涂层材料，以及纯度为 99.9% 的聚对二甲苯材料。实验设备包括精密电子天平、恒温恒湿箱、回流焊炉、二次离子质谱仪以及扫描电子显微镜。

B. 样品制备

根据 IPC/ JEDEC J-STD-033 联合行业标准，所有实验样品均在 125°C 下烘烤 24 小时以去除残余内部水分。随后，这些样品被随机分为三组：未保护组、纳米涂层组和聚对二甲苯涂层组。纳米涂层组采用浸渍-刷涂工艺：将电路板浸入纳米涂层溶液中 3 秒，随后在室温下固化 12 小时。该纳米涂层厚度相对较薄，在 SEM 观察下其形貌并不十分明显（如图 1 所示）。聚对二甲苯涂层组采用真空化学气相沉积工艺，在电路板表面沉积一层厚度约为 13 μm 的均匀薄膜。图 2 清晰展示了样品表面致密的聚对二甲苯薄膜。本研究中所述的后续实验步骤均在样品制备完成后 72 小时内完成。

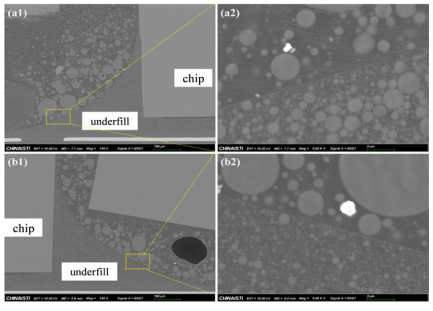

图 1. 纳米涂层的 SEM 形貌图：(a) 左侧；(b) 右侧。

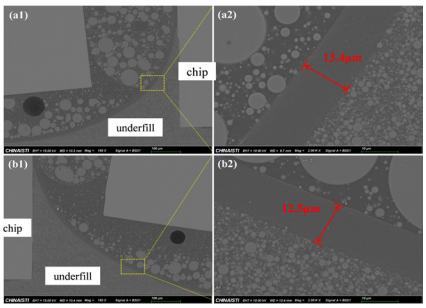

图 2. Parylene 涂层的 SEM 形貌图：(a) 左侧；(b) 右侧。

C. 试验方案

吸湿性测试：将三组样品置于温度为 85°C、相对湿度为 85% 的恒温恒湿试验箱中。使用精密电子天平测定质量变化。吸湿性测试时间安排如下：在初始 12 小时内，分别于 0 小时、1 小时、2 小时、4 小时、6 小时、8 小时、10 小时和 12 小时进行称重；在 12 小时至 204 小时期间，每 12 小时称重一次；204 小时后，每 24 小时称重一次，直至样品达到吸湿饱和状态。

D_2氘同位素示踪测试：将三组样品置于充满 D_2O 的 85°C/85% 相对湿度环境中共 1 小时。将样品从测试腔中取出后，从背面将基板研磨平整，直至露出基板下填充界面（如图 4 所示）。采用 ToFSIMS 技术对该界面进行分析，测量 H 和 D 离子浓度在 500 μm × 8000 μm 扫描区域内的分布情况。ToFSIMS 可检测样品中所有存在的 H 和 D 离子，包括来自样品组成分子的 H 和 D 离子，以及在 1 小时 HAST 测试期间扩散进入样品的 D 离子。在自然界中，D/H 比值约为 1.55×10^{-4}[6]。为隔离凸起结构对 D 离子信号扫描的影响，本系列实验需采用减小凸起结构的封装样品。仅在芯片四个角及中心处人工放置了 50 个凸起结构，其余所有封装工艺均保持一致。

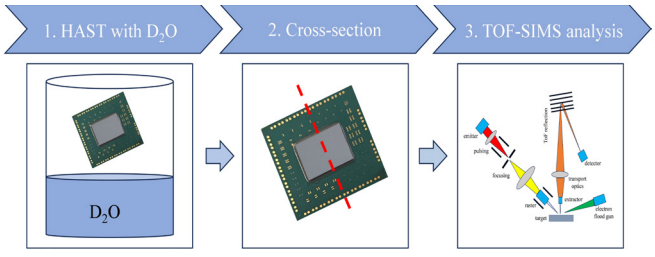

图 3.D_2氧同位素示踪法实验流程图。

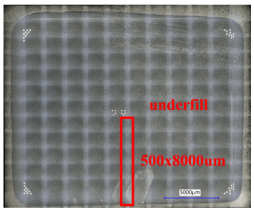

图 4. 扫描区域截面图。

MSL 1预处理与回流焊测试：根据 JEDEC J-STD-020 标准，三个样品组均进行了MSL 1预处理（85°C/85% RH，168小时）。在吸湿过程完成后4小时内，对样品进行了三次回流焊循环，峰值温度为260°C（±5°C）。

of 260°C (±5°C). The daisy-chain circuit was first tested for continuity using a multimeter. After removing the heat sink, scanning acoustic microscopy (SAM) was employed to inspect voids and delamination of the underfill. The substrate was ground to reduce thickness and then ultrasonically cut. SEM analysis was conducted to observe underfill cracking and the adhesion between the underfill and the substrate's solder mask layer.

III. RESULTS AND DISCUSSION

A. Moisture Absorption and Weight Gain Test Results

Fig. 5 displays the moisture absorption curves of the three samples over 420h. During the initial moisture diffusion phase (0–20h), the moisture absorption curves of the three samples exhibited similar trend with relatively rapid weight gain rate, showing no significant difference. This phenomenon indicates that during this stage, water molecules primarily penetrated through physical adsorption on the material surface and interfacial defects, with the protective layer not yet fully exerting its barrier function. As diffusion time extended (20–420h), the moisture absorption behavior of the three samples began to diverge markedly. The weight gain rate of the nano-coated sample decreased significantly, with a saturated moisture absorption rate of 0.207%, substantially lower than the other two groups. The unprotected sample exhibited the highest moisture absorption weight gain, reaching a saturated moisture absorption rate of 0.256%. The Parylene-coated sample achieved a saturated moisture absorption rate of 0.224%, positioned between the other two.

Diffusion kinetics analysis indicates that the initial rapid weight gain phase corresponds to physical adsorption and interfacial permeation processes, where moisture accumulates in micropores or nanopores, free volume, and at interfaces. The intermediate linear growth phase reflects volume diffusion-controlled mechanisms, while the subsequent slow weight gain phase indicates that moisture can still be absorbed through water-polymer affinity. This occurs due to the presence of hydrogen bonding sites along polymer chains and interfaces. Notably, even after 420h of testing, no significant moisture saturation plateau was observed in any sample, suggesting that moisture diffusion within the material is a continuous, slow process.

Microstructural analysis reveals that the superior performance of the nano-coating stems from its unique microstructural characteristics. In contrast, Parylene films exhibit a continuous, dense film structure that effectively blocks moisture diffusion pathways.

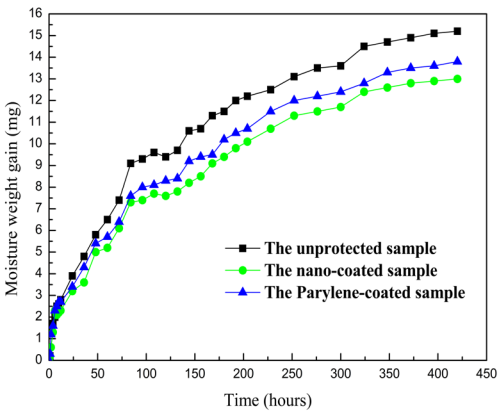

Fig. 5. Moisture Weight Gain Curve.

B. D_2O Isotope Tracing Test Results

Fig. 6 shows the D ion intensity at the substrate-underfill interface for unprotected samples after 1h of heavy water treatment at 85°C/85% RH. The average intensity is observed to be 0.1[7]. Fig. 7 displays the D ion intensity at the substrate -underfill interface for the nano-coated and the Parylene-coated samples. The average intensity values for both are relatively close, approximately 0.013, significantly lower than that of the unprotected sample. This indicates that both protective methods effectively block moisture diffusion into the circuit interior. The average intensity of D ion measured in the sample not treated with D_2O was determined in our other paper[7]. However, due to the minimal D ion diffusion into the protected samples in a relatively short period of time(only 1h), background noise in the intensity map persists, making it difficult to definitively compare their protective efficacy. Table 1 shows the H/D ion ratio within the scanned range, which is 6830 for the untreated sample. Three samples were taken for each type, and the test data represent the average values. This data indicates a lower D ion proportion in the nano-coated sample, suggesting that the nano-coating provides slightly superior barrier effectiveness.

TABLE I. H/D ION RATIO

Sample	H^-	D^-	H^-/D^- Ratio
The untreated sample	403000	59	6830
The unprotected sample, after D_2O 85℃/85%RH 1h	197000	167	1180
The Parylene-coated sample, after D_2O 85℃/85%RH 1h	242000	78	3461
The nano-coated sample, after D_2O 85℃/85%RH 1h	385000	82	4695

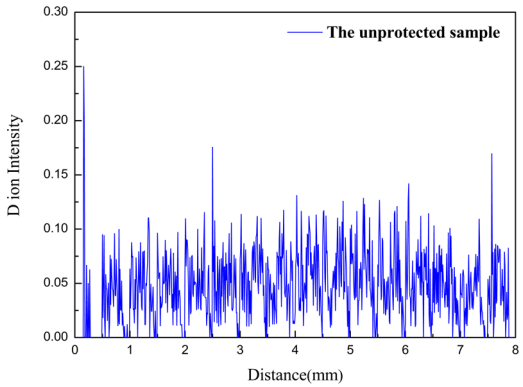

Fig. 6. D ion intensity profile of the unprotected sample at the substrate-underfill interface.

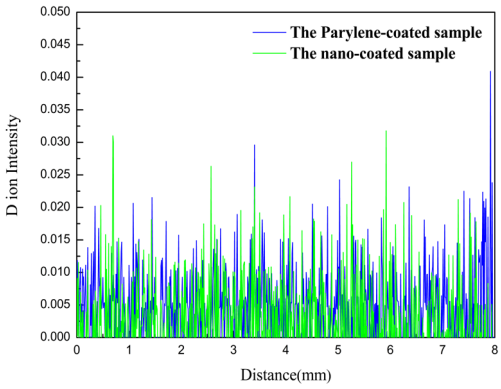

Fig. 7. D ion intensity profile of the nano-coated sample and the Paryene-coated sample at the substrate-underfill interface.

首先使用万用表对菊花链电路进行通断性测试；随后移除散热片，采用扫描声学显微镜（SAM）检测底填料中的空隙及分层现象；接着对基板进行研磨以减薄厚度，随后进行超声波切割；最后通过SEM分析观察底填料的开裂情况以及底填料与基板阻焊层之间的粘附性。

III. 结果与讨论

A. 吸湿与增重试验结果

图5展示了三种样品在420小时内的吸湿曲线。在初始水分扩散阶段（0–20小时），三种样品的吸湿曲线呈现相似趋势，且增重速率均相对较快，三者之间无显著差异；这一现象表明，在此阶段，水分子主要通过材料表面的物理吸附及界面缺陷进行渗透，此时保护层尚未充分发挥其阻隔作用。随着扩散时间延长（20–420小时），三种样品的吸湿行为开始出现明显差异：纳米涂层样品的增重速率显著降低，其饱和吸湿率仅为0.207%，明显低于另外两组样品；未涂层样品的吸湿增重最大，其饱和吸湿率达到0.256%；而Parylene涂层样品的饱和吸湿率为0.224%，介于上述两组之间。

扩散动力学分析表明，初始的快速增重阶段对应于物理吸附与界面渗透过程——在此过程中，水分积聚于微孔、纳米孔、自由体积及界面处；中间的线性增长阶段反映了受体积扩散控制的机制；而随后的缓慢增重阶段则表明，水分仍可通过水-聚合物间的亲和力被吸收——这归因于聚合物链及界面处存在的氢键作用位点。值得注意的是，即使经过 420 h 的测试，所有样品均未出现明显的水分饱和平台期，这表明材料内部的水分扩散是一个持续且缓慢的过程。

微观结构分析表明，该纳米涂层的优异性能源于其独特的微观结构特征；相比之下，聚对二甲苯薄膜则具有连续、致密的薄膜结构，可有效阻断水分扩散路径。

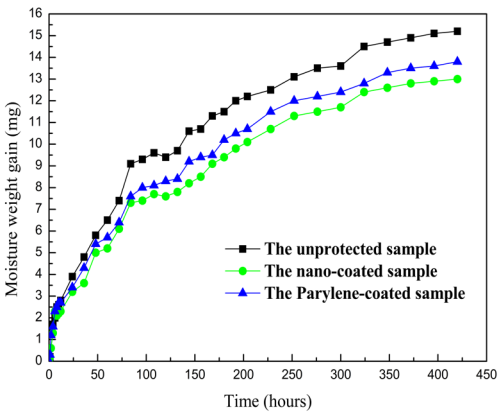

图 5. 湿重增加曲线。

B. D_2氧同位素示踪试验结果

图6展示了未经保护样品在85°C/85% RH条件下经1小时重水处理后，基材-底层填充界面处的D离子强度。观测到的平均强度为0.1[7]。图7显示了基材处的D离子强度。

-用于纳米涂层样品与Parylenecoated样品的底层界面分析。两者的平均强度值相对接近，约为0.013，显著低于未作保护处理的样品。这表明两种保护方法均能有效阻隔水分向电路内部的扩散。未经过D_2O处理的样品中测得的D离子平均强度值已在我们另一篇论文[7]中给出。然而，由于在相对较短的时间内（仅1小时）D离子向受保护样品中的扩散量极小，导致强度分布图中存在背景噪声，因此难以对这两种保护方法的防护效能进行明确比较。表1展示了扫描范围内H/D离子比值，未处理样品的该比值为6830。每种样品类型均取三个样本，测试数据代表平均值。该数据表明纳米涂层样品中的D离子比例较低，提示纳米涂层具有略优的阻隔效能。

表 I。　　H/D离子比

样本	H^-	D^-	H-/D-比值
未经处理的样品	403000	59	6830
未保护样品在D_2O 85℃/85%RH 条件下放置 1 小时后	197000	167	1180
经聚对二甲苯涂层处理的样品，在D_2O、85℃/85%RH 条件下处理 1 小时后	242000	78	3461
纳米涂层样品经D_2 85℃/85%相对湿度处理 1 小时后	385000	82	4695

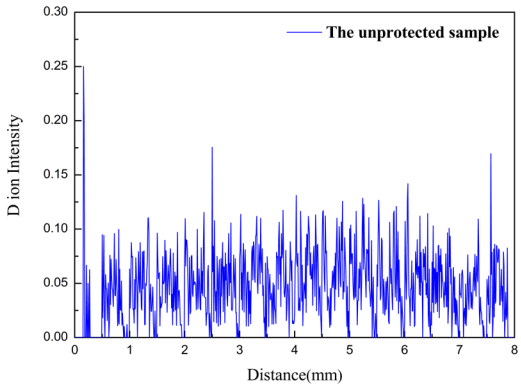

图 6. 未保护样品在基板下填充界面处的 D 离子强度分布曲线。

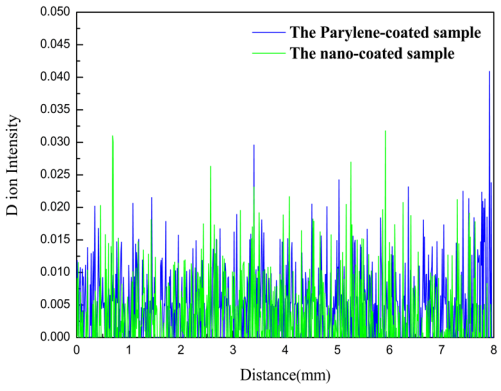

图 7. 纳米涂层样品与 Paryene 涂层样品在基材-底层填充界面处的 D 离子强度分布曲线。

C. *MSL 1 preconditioning and Reflow Soldering Test Results*

Non-preconditioned samples were selected as the baseline comparison group for this study. SAM images revealed uniform bright contrast in the underfill regions of all unassessed samples, indicating continuous ultrasonic wave propagation at material interfaces. Fig. 8 shows SEM images demonstrating tight bonding between the chip edge and underfill interface. The underfill completely filled the gap between the chip and substrate, establishing excellent contact. The underfill bonded well with the substrate's solder mask layer and the PI, showing no signs of delamination. Comprehensive inspection using SAT and SEM revealed outstanding interface integrity in this sample group, providing a benchmark reference for subsequent protective performance evaluation.

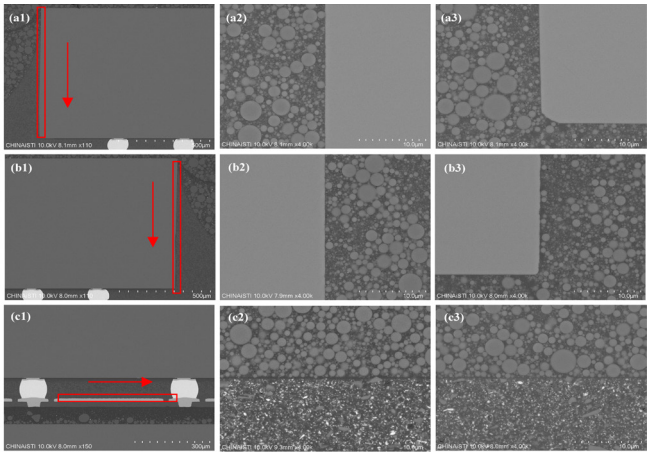

Fig. 8. SEM morphology image of the non-preconditioned sample. (a) Left side of the chip (b) Right side of the chip (c) Interface between underfill and solder mask layer, underfill and PI.

Unprotected and tested samples underwent daisy-chain electrical continuity testing, revealing that all samples maintained qualified electrical connections. SAT results at the underfill adhesive interface appeared normal. The sample was cut using ultrasonic waves at the position shown in Fig. 9. Subsequent sample dissection revealed no failure at the solder joints. However, SEM examination showed continuous delamination at the interface between the chip edge and the underfill. The upper width of the left crack was 1.79μm, increasing to 2.01μm at the lower section. The upper width of the right crack was 1.54μm, increasing to 1.95μm at the lower section, exhibiting a distinct gradient pattern. Crucially, cracking was observed within the core material of the underfill. This indicates material degradation occurred under the combined effects of hygrothermal stress.

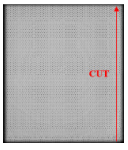

Fig. 9. SAT images of the unprotected sample and the cutting location.

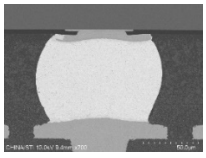

Fig. 10. SEM morphology image of the solder bump.

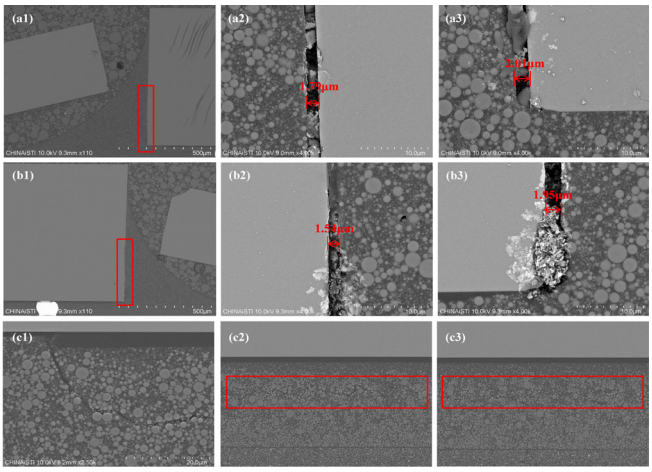

Fig. 11. SEM morphology image of the unprotected sample. (a) Left side of the chip (b) Right side of the chip (c) The underfill area.

The nano-coated sample and Parylene sample after evaluation showed no delamination at the interface between the chip edge and the underfill. The underfill itself maintained structural integrity without cracking, and no separation occurred at the bonding interfaces with the solder mask layer or PI. This indicates that both the nano-coating and Parylene-coating effectively blocked moisture penetration. During the high-temperature reflow soldering phase, the protective layers significantly reduced the moisture absorption of the underfill. Consequently, the internal vapor pressure generated by water vaporization was suppressed, preventing cracking of the underfill and interfacial delamination caused by pressure buildup. Nevertheless, it should be noted that while the protective layer primarily functions to block moisture, its ability to mitigate thermal stress caused by CTE mismatch between the chip and underfill is limited. If thermal stress exceeds the interfacial bond strength, localized damage may still occur; however, this did not constitute the dominant failure mode under the stress conditions of this experiment. These results underscore the critical role of moisture protection in maintaining the structural integrity of flip-chip circuits with organic substrate under high-temperature and high-humidity environment. They also provide experimental basis for subsequent composite material designs that balance moisture barrier with stress matching.

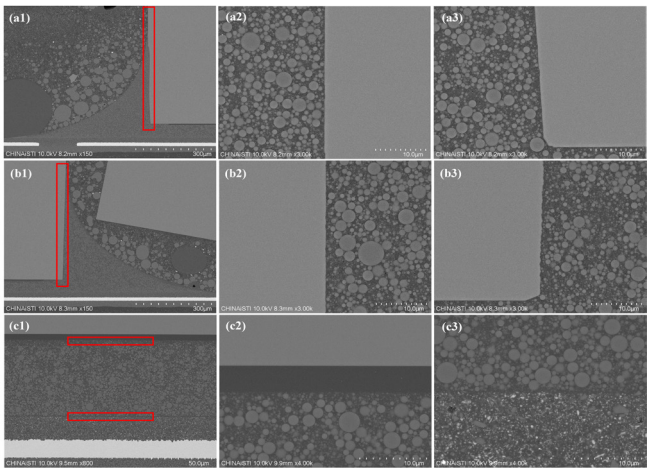

Fig. 12. SEM morphology image of the nano-coated sample. (a) Left side of the chip (b) Right side of the chip(c) Interface between underfill and solder mask layer, underfill and PI.

C. MSL-1预处理与回流焊测试结果

本研究选取未经预处理的样品作为基线对照组。SAM图像显示，所有未评估样品的填充层区域均呈现均匀的明亮对比度，表明超声波在材料界面处实现了连续传播。图8所示的SEM图像证实了芯片边缘与填充层界面之间存在紧密结合。该填充层完全填满了芯片与基板之间的间隙，从而建立了优异的接触界面；同时，该填充层与基板的阻焊层及PI材料均结合良好，未出现分层现象。通过SAT与SEM技术进行的全面检测表明，该样品组具有卓越的界面完整性，为后续的保护性能评估提供了基准参考。

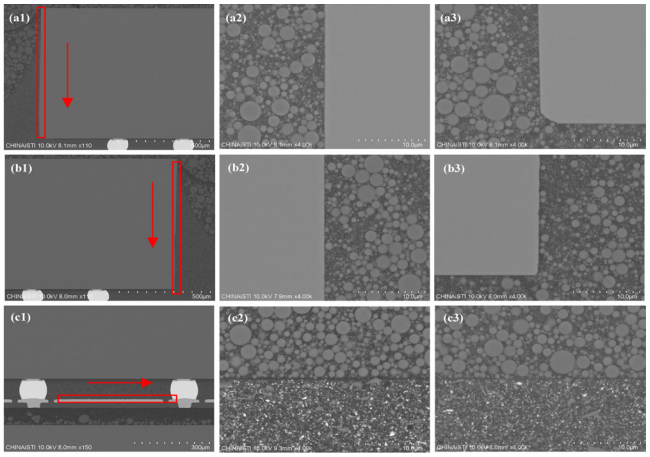

图 8. 未经预处理样品的 SEM 形貌图像：(a) 芯片左侧；(b) 芯片右侧；(c) 填充料与阻焊层、填充料与 PI 之间的界面。

未经保护且经过测试的样品接受了菊花链式电气连通性测试，结果表明所有样品均保持合格的电气连接状态；底填胶界面处的SAT检测结果亦显示正常。该样品在图9所示位置采用超声波进行切割；随后对样品进行剖面分析，未发现焊点存在失效现象。然而，SEM检测显示，在芯片边缘与底填胶之间的界面处存在连续的分层现象：左侧裂纹的上部宽度为1.79 μm，下部宽度增至2.01 μm；右侧裂纹的上部宽度为1.54 μm，下部宽度增至1.95 μm，呈现出明显的梯度变化趋势。尤为关键的是，在底填胶的芯材内部观察到了裂纹现象，这表明材料在湿热应力的共同作用下发生了劣化。

图 9. 未防护样品与切割部位的 SAT 图像。

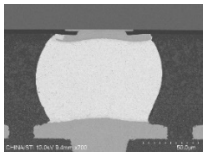

图 10. 焊料凸点的 SEM 形态学图像。

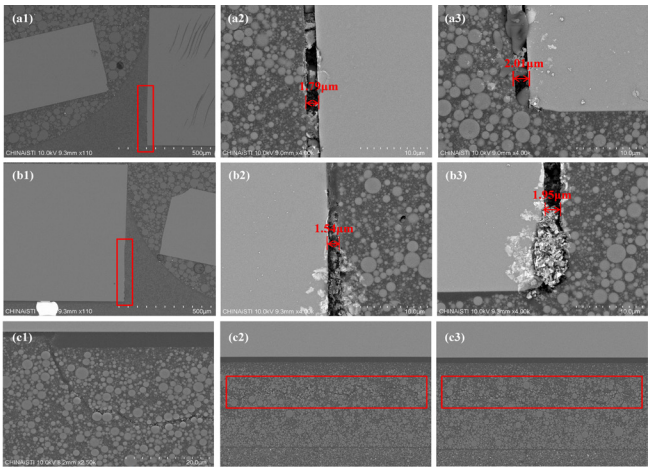

图 11. 未防护样品的 SEM 形貌图像：(a) 芯片左侧；(b) 芯片右侧；(c) 填充区。

经评估，纳米涂层样品与聚对二甲苯涂层样品在芯片边缘与底层填充材料之间的界面均未出现分层现象；底层填充材料本身保持了结构完整性且未出现开裂；在与阻焊层或PI材料的结合界面处亦未发生分离。这表明纳米涂层与聚对二甲苯涂层均能有效阻隔水分渗透。在高温回流焊工艺阶段，这些保护层显著降低了底层填充材料的吸湿量；因此，由水蒸气汽化产生的内部蒸汽压得到抑制，从而避免了因压力积聚导致的底层填充材料开裂或界面分层现象。然而需注意的是，尽管该保护层主要作用在于阻隔水分，但其缓解芯片与底层填充材料之间热膨胀系数（CTE）不匹配所引发的热应力的能力有限。若热应力超过界面结合强度，仍可能发生局部损伤；但在本实验所采用的应力条件下，此类损伤并非主导性失效模式。这些结果凸显了防潮保护在高温高湿环境下维持采用有机基材的倒装芯片电路结构完整性中的关键作用；同时，也为后续设计兼顾防潮性能与应力匹配的复合材料提供了实验依据。

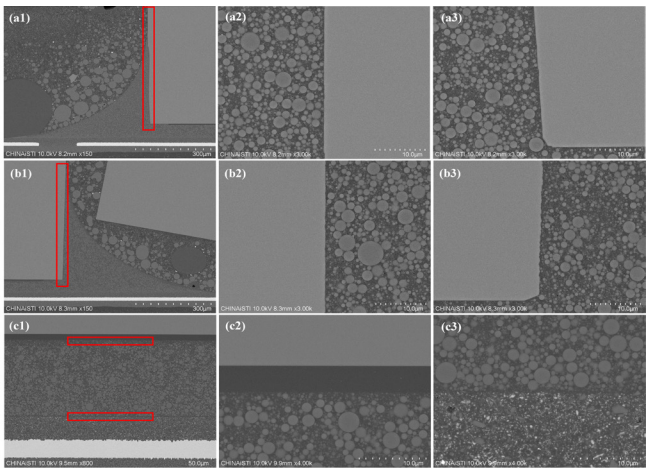

图 12. 纳米涂层样品的 SEM 形貌图像：(a) 芯片左侧；(b) 芯片右侧；(c) 下填充料与阻焊层之间的界面，以及下填充料与 PI 之间的界面。

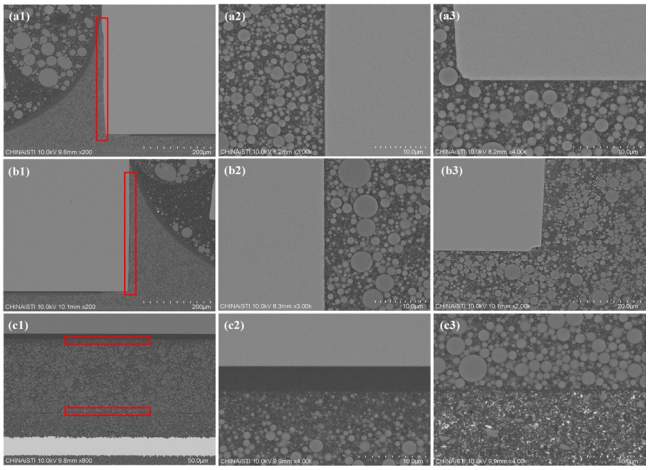

Fig. 13. SEM morphology image of the Parylene-coated sample. (a) Left side of the chip (b) Right side of the chip (c) Interface between underfill and solder mask layer, underfill and PI.

IV. CONCLUSION

This study systematically compared the effectiveness of the nano-coated and Parylene-coated technologies for moisture barrier in flip-chip circuits on organic substrates. Comprehensive evaluations of protective performance were conducted through moisture absorption weight gain tests, heavy water tracing, and MSL 1 preconditioning combined with reflow soldering tests. Key findings include:

(1) Moisture absorption test revealed that the nano-coated sample exhibited optimal moisture resistance, with a saturated moisture absorption rate of only 0.207%. This was significantly lower than the Parylene-coated sample (0.224%) and unprotected samples (0.256%). The moisture uptake kinetics of all three samples exhibited a rapid initial moisture ingress rate followed by gradual deceleration. The protective treatment did not alter the fundamental diffusion mechanism of moisture within the material but effectively enhanced the barrier effect.

(2) D_2O isotope tracing test results showed that both the nano-coating and Parylene-coating significantly suppressed D ion permeation, with an average signal intensity of approximately 0.013—one order of magnitude lower than the unprotected sample (0.1). Based on the hydrogen/deuterium ratio, the nanocoated sample exhibited a lower proportion of D ion, indicating slightly superior protective performance compared to the Parylene-coating.

(3) After MSL Level 1 preconditioning and three 260°C reflow soldering cycles, the unprotected sample exhibited delamination at the substrate-underfill interface and cracking within the underfill. Both protected samples show no microcracks at the interface, no cracking occurred within the underfill and no separation occurred at the interfaces with the solder mask layer or PI. Results indicate that protective treatment effectively blocks moisture ingress and inhibits material hydrolysis.

In summary, the nano-coating demonstrated slightly superior overall moisture resistance and impermeability compared to the Parylene-coating, particularly exhibiting better interface integrity maintenance in environments with coupled high humidity and thermal loading. This study provides experimental evidence and theoretical support for the protective design of high-density plastic-encapsulated flip-chip circuits in humid-heat environments.

ACKNOWLEDGMENT

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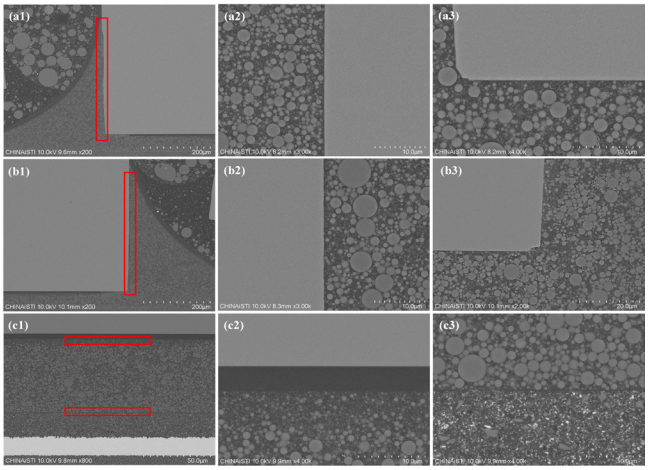

图 13. Parylene 涂层样品的 SEM 形貌图像。(a) 芯片左侧；(b) 芯片右侧；(c) 下填充料与阻焊层、下填充料与 PI 之间的界面。

IV. 结论

本研究系统比较了纳米涂层与聚对二甲苯涂层技术在有机基板上的倒装芯片电路中作为防潮层的有效性。通过吸湿增重测试、重水示踪法以及MSL 1预处理结合回流焊测试，对防护性能进行了全面评估。主要研究结果如下：

(1) 吸湿性测试表明，纳米涂层样品具有最佳的耐湿性，其饱和吸湿率仅为 0.207%；这一数值显著低于聚对二甲苯涂层样品（0.224%）及未涂层样品（0.256%）。三种样品的吸湿动力学曲线均呈现初始吸湿速率较快、随后逐渐放缓的趋势。该保护性处理并未改变材料内部水分的基本扩散机制，但有效增强了其阻湿性能。

(2) D_2同位素示踪测试结果表明，纳米涂层与聚对二甲苯涂层均能显著抑制 D 离子渗透，其平均信号强度约为 0.013——比未处理样品（0.1）低一个数量级。根据氢/氘比值分析，纳米涂层样品中的 D 离子占比较低，表明其防护性能略优于聚对二甲苯涂层。

(3) 经过MSL Level 1预处理及三次260°C回流焊循环后，未受保护的样品在基材-底层灌封界面处出现分层现象，且底层灌封内部出现裂纹；而两个受保护的样品在界面处均未出现微裂纹，底层灌封内部未发生裂纹，且与阻焊层或PI层的界面处均未出现分离现象。结果表明，保护性处理能有效阻隔水分侵入并抑制材料水解。

综上所述，与聚对二甲苯涂层相比，该纳米涂层在整体耐湿性和防水性方面均略胜一筹，尤其在同时存在高湿度与热载荷的环境中，能更好地维持界面完整性。本研究为在高湿热环境下对高密度塑料封装倒装芯片电路进行防护设计提供了实验依据与理论支持。

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